

FIG. 3A

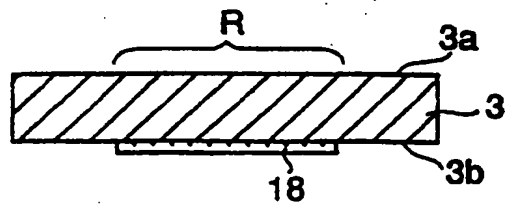


FIG. 3B

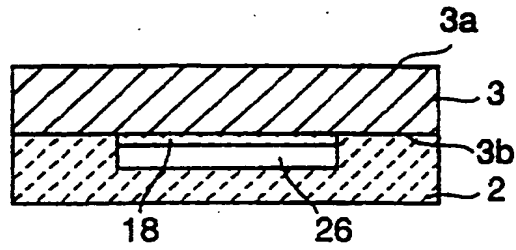


FIG. 3C

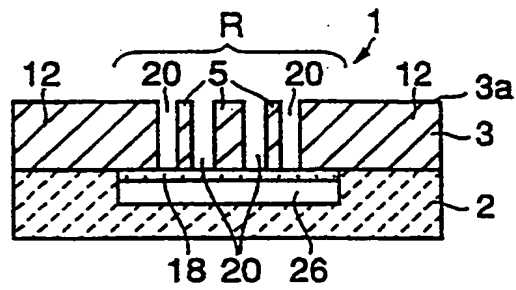


FIG. 3D

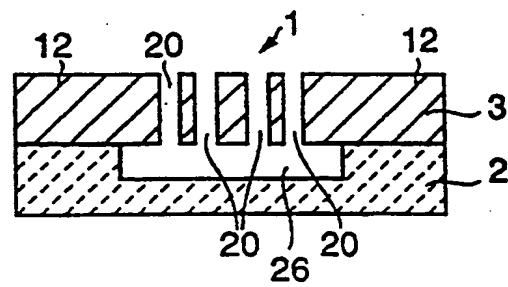


FIG. 4A

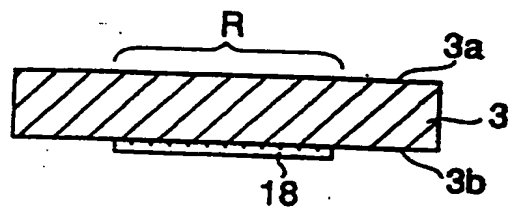


FIG. 4B

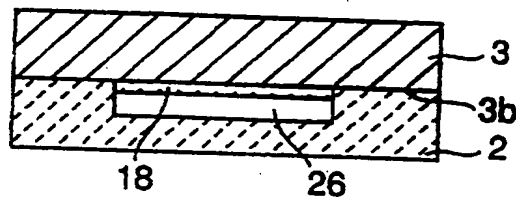


FIG. 4C

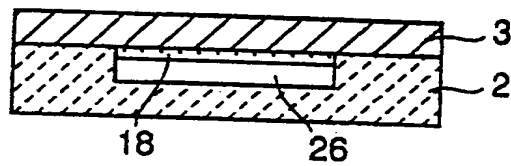


FIG. 4D

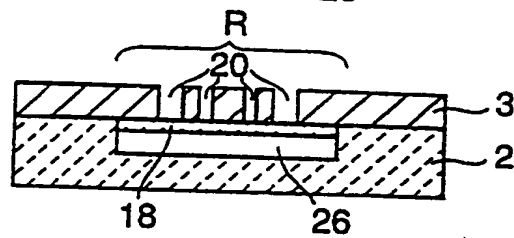


FIG. 4E

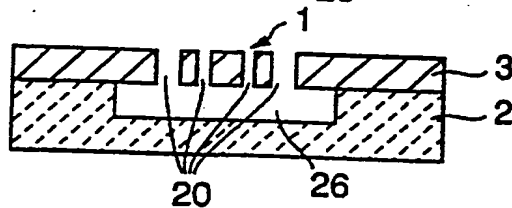


FIG. 5A

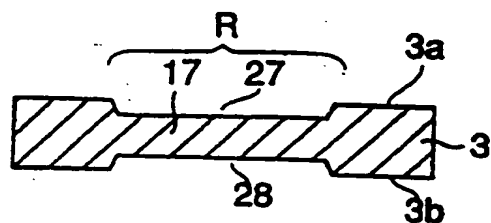


FIG. 5B

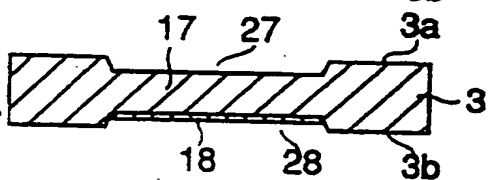


FIG. 5C

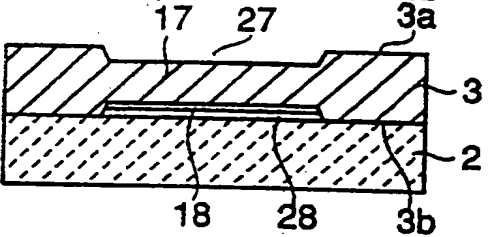


FIG. 5D

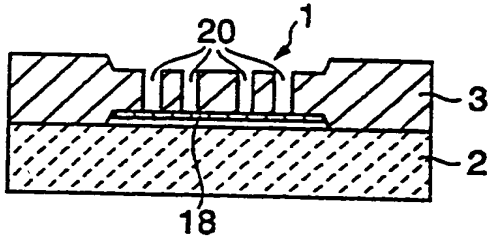


FIG. 5E

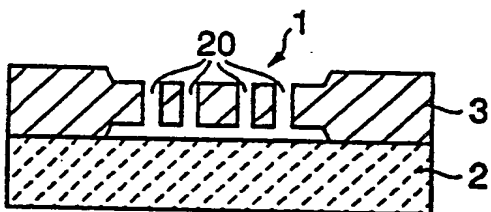


FIG. 6A

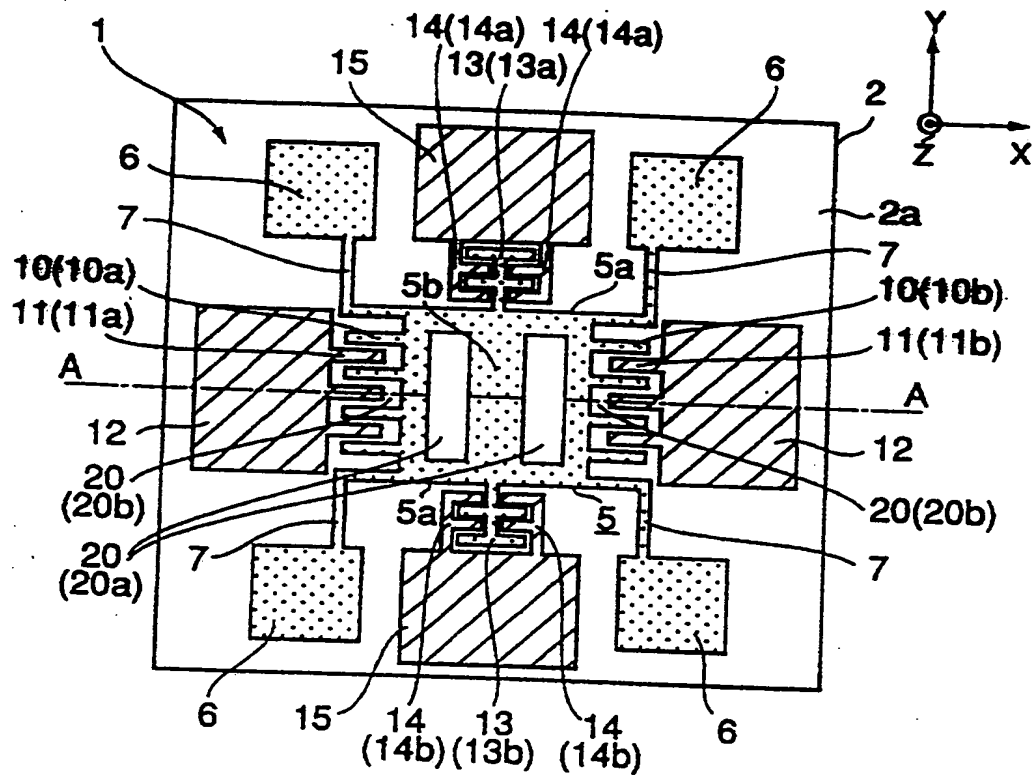
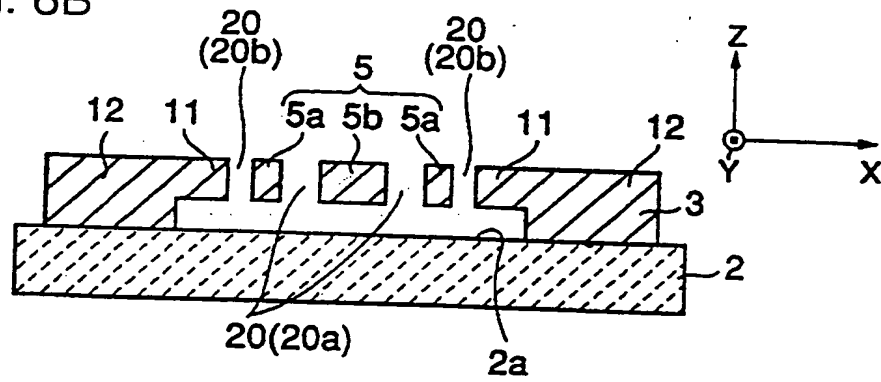


FIG. 6B



This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 3 with a central layer 16. A layer 17 is formed on top of layer 16, with a thickness indicated by 'd'. The layer 17 is wider than the central portion of layer 16, extending over the side regions of the substrate 3, which are labeled 3b.

A cross-sectional view of a substrate 3 with a conductive layer 2. A conductive pad 16 is formed on the conductive layer 2. A conductive pad 18 is formed on the conductive layer 2.

FIG. 8A
PRIOR ART

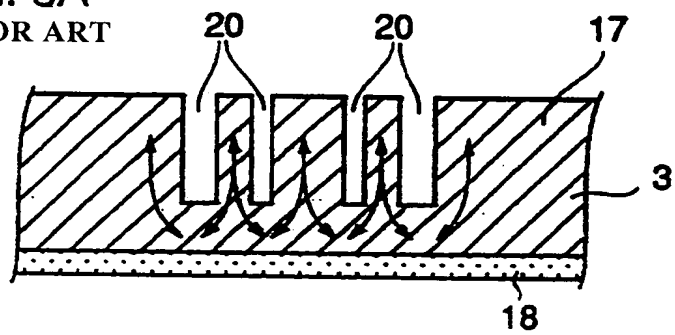


FIG. 8B
PRIOR ART

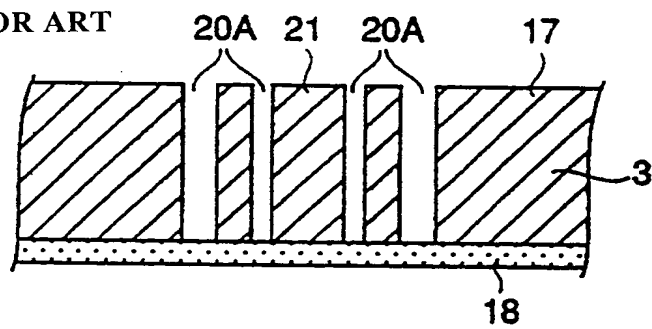


FIG. 8C
PRIOR ART

